WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

an insulating substrate;

a plurality of first signal lines formed on the insulating substrate;

a plurality of second signal lines formed on the insulating substrate, insulated from the first signal lines, and intersecting the first signal lines;

a plurality of pixel electrodes provided on the respective pixel areas defined by the intersections of the first and the second signal lines, each pixel electrode having a cutout;

a plurality of direction control electrodes provided on the respective pixel areas defined by the intersections of the first and the second signal lines;

a first thin film transistor connected to a relevant one of the first signal lines, a relevant one of the second signal lines and a relevant one of the pixel electrodes;

a second thin film transistor connected to a previous one of the first signal lines, a previous one of the second signal lines and a relevant one of the direction control electrodes; and

a third thin film transistor connected to the previous first signal line, the relevant second signal line and the relevant pixel electrode.

2. The thin film transistor array panel of claim 1, further comprising a third signal line insulated from the second signal lines and intersecting the second signal lines, the third signal line including a portion overlapping the cutout of the pixel electrode.

3. A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate and including first to third gate electrodes and a plurality of gate lines;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the semiconductor layer and including a plurality of data lines intersecting the gate lines, first to third source electrodes connected to the

data lines, and first to third drain electrodes opposite the first to the third source electrodes with respect to the first to the third gate electrodes;

a direction control electrode connected to the second drain electrode;

a protective layer formed on the data wire and the direction control electrode and having a plurality of contact holes; and

a pixel electrode formed on the protective layer, having a plurality of cutouts, and electrically connected to the first and the third drain electrodes through the contact holes.

4. The thin film transistor array panel of claim 3, wherein the first and the third source electrodes are connected to a relevant one of the data lines, the second source electrode is connected to a previous one of the data lines, the first and the second gate electrodes are connected to a previous one of the gate lines, and the third gate electrode is connected to a relevant one of the gate lines.

5. The thin film transistor array panel of claim 4, wherein the cutouts of the pixel electrode comprise a transverse cutout bisecting the pixel electrode 190 into upper and lower halves and a plurality of oblique cutouts having inversion symmetry with respect to the transverse cutout.

6. The thin film transistor array panel of claim 4, wherein the direction control electrode overlaps at least one of the cutouts of the pixel electrode and has inversion symmetry with respect to a transverse one of the cutouts of the pixel electrode.

7. The thin film transistor array panel of claim 4, further comprising a storage electrode wire including substantially the same layer as the gate wire and having a portion overlapping at least one of the cutouts of the pixel electrode.

8. The thin film transistor array panel of claim 4, wherein the direction control electrode includes substantially the same layer and material as the data wire.

9. The thin film transistor array panel of claim 4, wherein the contact holes have rectangular shapes having an edge parallel to or perpendicular to the oblique cutouts.

10. The thin film transistor array panel of claim 4, wherein the data wire and the direction control electrode include double layers of a semiconductor layer and a metal layer.

11. The thin film transistor array panel of claim 4, wherein the semiconductor layer includes double films of an amorphous silicon film and an ohmic contact layer.

12. A liquid crystal display comprising:

a first insulating substrate;

a plurality of first signal lines formed on the first insulating substrate;

a plurality of second signal lines formed on the first insulating substrate, insulated from the first signal lines, and intersecting the first signal lines;

a plurality of pixel electrodes provided on the respective pixel areas defined by the intersections of the first and the second signal lines, the pixel electrodes having cutouts;

a plurality of direction control electrodes provided on the respective pixel areas defined by the intersections of the first and the second signal lines;

a first thin film transistor connected to a relevant one of the first signal lines, a relevant one of the second signal lines and a relevant one of the pixel electrodes;

a second thin film transistor connected to a previous one of the first signal lines, a previous one of the second signal lines and a relevant one of the direction control electrodes;

a third thin film transistor connected to the previous first signal line, the relevant second signal line and the relevant pixel electrode;

a second insulating substrate opposite the first insulting substrate;

a common electrode formed on the second insulating substrate; and

a liquid crystal layer interposed between the first and the second substrates.

13. The liquid crystal display of claim 12, wherein the liquid crystal layer has negative dielectric anisotropy and major axes of liquid crystal molecules in the liquid crystal layer are aligned vertical to the first and the second substrates.